REMARKS

This application has been carefully reviewed in light of the Office Action dated April 17, 2006. Claims 1 to 11 have been cancelled herein, without prejudice or disclaimer of subject matter, and claims 12 to 24 have been added, of which claims 12, 13, 19 and 20 are the independent claims. No new matter has been added. Reconsideration and further examination are respectfully requested.

Initially, the Examiner's indication that claims 3 and 9 contain allowable subject matter is acknowledged with appreciation. In response, and accordance with the Examiner's suggestion, the substance of allowable claim 3 has been rewritten in independent form as independent claim 13, and the substance of allowable claim 9 has been rewritten in independent form as independent claim 20. Accordingly, independent claims 13 and 20, and dependent claims 14 to 18 and 21 to 24 are believed to be allowable over the applied references.

In the Office Action, claims 1, 5, 7 and 11 were rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,831,700 ("Hoshikawa"); and claims 2, 4, 6, 8 and 10 were rejected under 35 U.S.C. § 103(a) over Hoshikawa in view of U.S. Patent No. 6,636,269 ("Baldwin"). As indicated above, claims 1 to 11 have been cancelled herein, without prejudice or disclaimer of subject matter, and without conceding the correctness of the rejections. Withdrawal of the rejections and further examination are respectfully requested.

According to one general implementation, the present disclosure generally relates to processing a video signal utilizing a video signal processing apparatus which includes a plurality of line memories to which in-sequence video signal data inputted is written on a line-by-line basis, a timing controller operable to control a timing to write the video signal data to the plurality of line memories and to control a timing to read the video signal data from the plurality of line memories, and a computation output portion operable to compute the video signal data read from the plurality of line memories and to output video signal data differing in resolution which is determined by a pixel count in the horizontal direction and a line count in the vertical direction. A reference pixel count is determined in the horizontal direction of the video signal data obtained from the computation output portion on the basis of a difference between an elapsed period of time for a specified number of lines of the video signal data inputted and an

elapsed period of time for a line count corresponding to the specified number of lines of the video signal data obtained from the computation output portion, where the difference is also determined depending on a conversion rate of the resolution of the video signal data. For a partial line of one screen-full of lines in the vertical direction of the video signal data obtained from the computation output portion, the reference pixel count is varied from the pixel count in the horizontal direction of the video signal data making up the partial line, depending on the conversion rate of the resolution of the video signal data.

Referring to particular claim language, independent claim 12 recites a video signal processing apparatus including a plurality of line memories to which in-sequence video signal data inputted is written on a line-by-line basis and a timing controller operable to control a timing to write the video signal data to the plurality of line memories, and to control a timing to read the video signal data from the plurality of line memories. The video signal processing apparatus also includes a computation output portion operable to compute the video signal data read from the plurality of line memories, and to output video signal data differing in resolution which is determined by a pixel count in the horizontal direction and a line count in the vertical direction, and a reference pixel count decision unit operable to determine a reference pixel count in the horizontal direction of the video signal data obtained from the computation output portion based on a difference between an elapsed period of time for a specified number of lines of the video signal data inputted and an elapsed period of time for a line count corresponding to the specified number of lines of the video signal data obtained from the computation output portion, wherein the difference is also determined depending on a conversion rate of a resolution of the video signal data. The video signal processing apparatus also includes a pixel count variation unit operable to vary, for a partial line of one screen-full of lines in the vertical direction of the video signal data obtained from the computation output portion, from the reference pixel count, the pixel count in the horizontal direction of the video signal data making up the partial line, depending on the conversion rate of the resolution of the video signal data.

Independent claim 19 recites a method of processing a video signal for a video signal processing apparatus which includes a plurality of line memories to which in-sequence video signal data inputted is written on a line-by-line basis, a timing controller operable to control a timing to write the video signal data to the plurality of line memories and to control a timing to

read the video signal data from the plurality of line memories, and a computation output portion operable to compute the video signal data read from the plurality of line memories and to output video signal data differing in resolution which is determined by a pixel count in the horizontal direction and a line count in the vertical direction. The method of processing the video signal includes determining a reference pixel count in the horizontal direction of the video signal data obtained from the computation output portion on the basis of a difference between an elapsed period of time for a specified number of lines of the video signal data inputted and an elapsed period of time for a line count corresponding to the specified number of lines of the video signal data obtained from the computation output portion, where the difference is also determined depending on a conversion rate of the resolution of the video signal data. The method also includes varying, for a partial line of one screen-full of lines in the vertical direction of the video signal data obtained from the computation output portion, from the reference pixel count, the pixel count in the horizontal direction of the video signal data making up the partial line, depending on the conversion rate of the resolution of the video signal data.

The applied art is not seen to disclose, teach or to suggest the foregoing features recited by the independent claims. In particular, Hoshikawa is not seen to disclose at least the features that *i)* a reference pixel count is determined in the horizontal direction of the video signal data obtained from the computation output portion on the basis of a difference between an elapsed period of time for a specified number of lines of the video signal data inputted and an elapsed period of time for a line count corresponding to the specified number of lines of the video signal data obtained from the computation output portion, where the difference is also determined depending on a conversion rate of the resolution of the video signal data and *ii)* for a partial line of one screen-full of lines in the vertical direction of the video signal data obtained from the computation output portion, the reference pixel count is varied from the pixel count in the horizontal direction of the video signal data making up the partial line, depending on the conversion rate of the resolution of the video signal data.

To its advantage, the present disclosure provides for reliably writing to and reading from a plurality of line memories following a change of the conversion rate of the resolution of the video signal data. More particularly, a reversal of the writing to and reading from the plurality of the line memories can be prevented, effectively preventing disturbances within a screen image.

Hoshikawa is seen to describe a video signal processor capable of varying a resolution of image displayed on a display. *See* Hoshikawa, Abstract. The video signal processor includes a horizontal resolution processor 22 which generates a video data series D_{CH} with a changed horizontal resolution of a video data series D_C, three line memories 27, 28, 29 for writing and reading the video data series D_{CH}, and a mixer 9 which combines appropriately the video data series D_{CH} read selectively from the line memories 27, 28, 29 to generate a video data series D_{HV}. *See* Hoshikawa, Accordingly, while it is true that the video signal processor can vary a resolution of video data in the horizontal and vertical directions, it is also true that the pixel count in the horizontal direction is merely varied homogeneously by converting the resolution of the video data. Accordingly, Hoshikawa is not seen to describe, nor does the Office Action even allege that Hoshikawa describes, at least the features that *i)* a reference pixel count is determined in the horizontal direction of the video signal data obtained from the computation output portion on the basis of a difference between an elapsed period of time for a specified number of lines of the video signal data inputted and an elapsed period of time for a line count corresponding to the specified number of lines of the video signal data obtained from the computation output portion, where the difference is also determined depending on a conversion rate of the resolution of the video signal data and *ii)* for a partial line of one screen-full of lines in the vertical direction of the video signal data obtained from the computation output portion, the reference pixel count is varied from the pixel count in the horizontal direction of the video signal data making up the partial line, depending on the conversion rate of the resolution of the video signal data.

Based on the foregoing amendments and remarks, independent claims 12 and 19 are believed to be allowable over the applied references. The other rejected claims in the application each contain allowable subject matter, or are each dependent from the independent claims and are believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define additional aspects of the disclosure, however, the individual consideration of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

The fee in the amount of $200.00 for the excess claim fee is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06 1050.

Respectfully submitted,

Date: July 17, 2006

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